Audio Processor

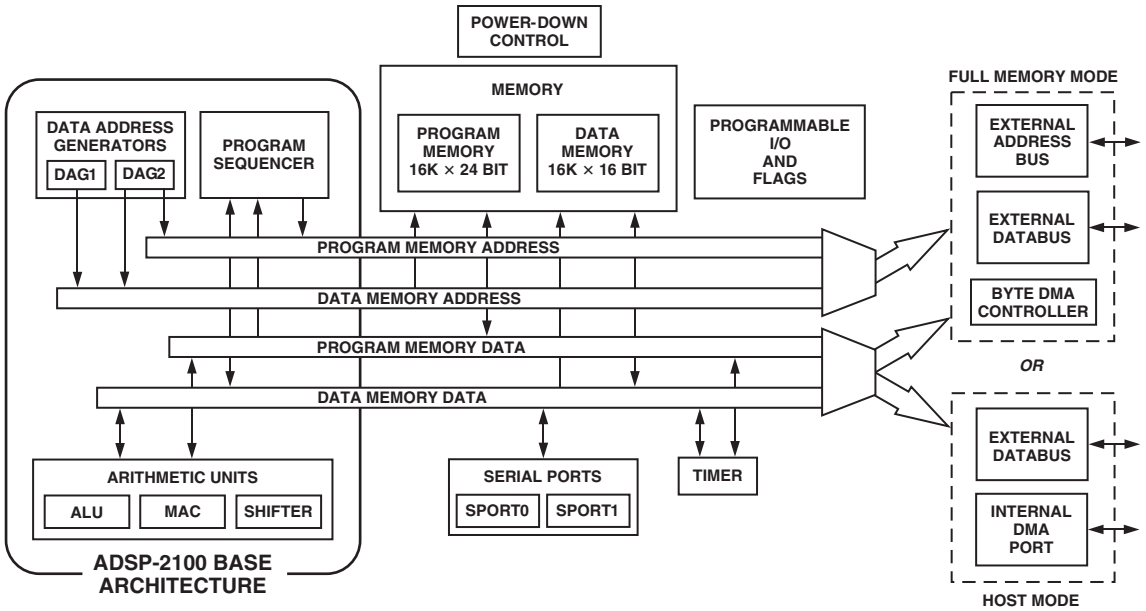
SST-Melody®-DAP

FEATURES

- 16-Bit Fixed-Point Audio Processor (DSP-Based)
- Decodes Major Standard Audio Formats Using 16-Bit Fixed-Point Implementation for Decoding:
  - MPEG 1 Layer I, II, and III (MP3)
  - AAC 2-Channel Low Complexity
  - Microsoft WMA
  - Speech Codecs: MGSM, G.723.1, and Audible Audio
- 2 Independent Data Address Generators
- Powerful Program Sequencer Provides Zero Overhead Looping Conditional Instruction Execution Programmable 16-Bit Interval Timer with Prescaler 100-Lead LQFP and 144-Ball Mini-BGA
- Supports Postprocessing:
  - Jazz/Rock/Classic/Pop/Bass
  - 3-Band User Customizable Graphic Equalizer
- Supports Major Storage Formats:
  - SmartMedia Card
  - DataPlay
  - SD Card
  - NAND Flash
- Supports DRM (Digital Rights Management) Technologies:
  - Liquid Audio SP3
  - Microsoft DRM
  - DataPlay ContentKey
- Supports Standard APIs:
  - Start Play
  - Stop Play
  - Mute Play
  - Resume Play
  - Download Song to Flash
  - Forward to Next Song
  - Rewind to Previous Song
  - Delete a Song
  - Bass/Equalizer
  - Erase MP3 Flash
  - Upload Song/Voice from Flash
  - Rename Flash
  - Start Record
  - Stop Record
  - Report
  - Get File Information
  - Seek File
  - List Number of Songs
  - Request Song Name
  - List Number of Voices
  - Request Voice Note Name
  - Start Record (G.723.1)
  - Stop Record (G.723.1)
  - Start Play (G.723.1)
  - Stop Play (G.723.1)

(continued on page 2)

FUNCTIONAL BLOCK DIAGRAM



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

- Mute Play (Voice)
- Resume Play (Voice)
- Download Voice to Flash
- Forward to Next Record
- Rewind to Previous Record
- Delete a Record
- Erase Voice Flash
- Version Reporting (G.723.1)
- Get G.723.1 Record Information
- Rename Voice File
- Format Flash
- Volume Control
- Get Song Name
- Get Album Name
- Get Singer Name
- Get Song Duration
- Version Reporting

Supports PC Interface
- USB 1.1 Interface
- Parallel Port Interface

Other Features:
- ID3 Tag Support
- SDMI Capable

PERFORMANCE

13.3 ns Instruction Cycle Time @ 2.5 V (Internal)
75 MIPS Sustained Performance
Single-Cycle Instruction Execution
Single-Cycle Context Switch
3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
Multifunction Instructions
Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 200 CLKIN Cycle Recovery from Power-Down Condition
Low Power Dissipation in Idle Mode

INTEGRATION

ADSP-2100 Family Code Compatible (Easy to Use Algebraic Syntax), with Instruction Set Extensions
80 Kbytes of On-Chip RAM, Configured as 16K Words Program Memory RAM
16K Words Data Memory RAM
Dual-Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units

SYSTEM INTERFACE

Flexible I/O Structure Allows 2.5 V or 3.3 V Operation; All Inputs Tolerate up to 3.6 V Regardless of Mode
16-Bit Internal DMA Port for High Speed Access to On-Chip Memory (Mode Selectable)
4 MByte Memory Interface for Storage of Data Tables and Program Overlays (Mode Selectable)
8-Bit DMA to Byte Memory for Transparent Program and Data Memory Transfers (Mode Selectable)
I/O Memory Interface with 2048 Locations Supports Parallel Peripherals (Mode Selectable)
Programmable Memory Strobe and Separate I/O Memory Space Permits “Glueless” System Design
Programmable Wait State Generation
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory, e.g., EPROM, or through Internal DMA Port
Six External Interrupts
13 Programmable Flag Pins Provide Flexible System Signaling
UART Emulation through Software SPORT Reconfiguration
ICE-Port™ Emulator Interface Supports Debugging in Final Systems

ICE-Port is a trademark of Analog Devices, Inc.

TABLE OF CONTENTS

Tables

SST-Melody-DAP

GENERAL DESCRIPTION

The SST-Melody-DAP is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

The SST-Melody-DAP combines the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The SST-Melody-DAP integrates 80 Kbytes of on-chip memory configured as 16K words (24-bit) of program RAM, and 16K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. The SST-Melody-DAP is available in a 100-lead LQFP package and 144-ball mini-BGA.

In addition, the SST-Melody-DAP supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (x squared), biased rounding, result-free ALU operations, I/O memory transfers, and global interrupt masking, for increased flexibility. Fabricated in a high speed, low power, CMOS process, the SST-Melody-DAP operates with a 13.3 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The SST-Melody-DAP's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, the SST-Melody-DAP can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

Instruction Set Description

The SST-Melody-DAP assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability.

The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the SST-Melody-DAP's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

	K Grade		B Grade		
Parameter	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{DDINT}	2.37	2.63	2.25	2.75	V
V_{DDEXT}	2.37	3.6	2.25	3.6	V
V_{INPUT}	V_{IL} = –0.3	V_{IH} = +3.6	V_{IL} = –0.3	V_{IH} = +3.6	V
T_{AMB}	0	+70	–40	+85	°C

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DDINT} = max	1.5			V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DDINT} = max	2.0			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DDINT} = min			0.7	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OH} = –0.5 mA	2.0			V
		@ V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
		@ V_{DDEXT} = min, I_{OH} = –100 mA[6]	V_{DDEXT} – 0.3			V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 2.5, t_{CK} = 15 ns		9		mA
		@ V_{DDINT} = 2.5, t_{CK} = 13.3 ns		10		mA
I_{DD}	Supply Current (Dynamic)[9]	@ V_{DDINT} = 2.5, 15 ns[10], T_{AMB} = 25°C		35		mA
		@ V_{DDINT} = 2.5, 13.3 ns[10], T_{AMB} = 25°C		38		mA
I_{DD}	Supply Current (Power-Down)[11]	@ V_{DDINT} = 2.5, T_{AMB} = 25°C in Lowest Power Mode		100		µA
C_I	Input Pin Capacitance[3, 6]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 11, 12]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF

NOTES

[1]Bidirectional pins: D0–D3, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$

[5]Although specified for TTL outputs, all ADSP-2185M outputs are CMOS compatible and will drive to V_{DDEXT} and GND, assuming no dc loads.

[6]Guaranteed but not tested

[7]Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7

[8]0 V on $\overline{\text{BR}}$

[9]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunctional (types 1, 4, 5, 12, 13, 14), 30% are type 2 and type 6, and 20% are idle instructions.

[10]V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[11]See Chapter 9 of the *ADSP-2100 Family User's Manual* (3rd Edition, 9/95) for details.

[12]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Internal Supply Voltage (V_{DDINT}) . . . . . –0.3 V to +3.0 V
Internal Supply Voltage (V_{DDEXT}) . . . . . –0.3 V to +4.0 V
Input Voltage[2] . . . . . –0.5 V to +4.0 V
Output Voltage Swing[3] . . . . . –0.5 V to V_{DDEXT} + 0.5 V
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) LQFP . . . . . 280°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Applies to bidirectional pins (D0–D3, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$)

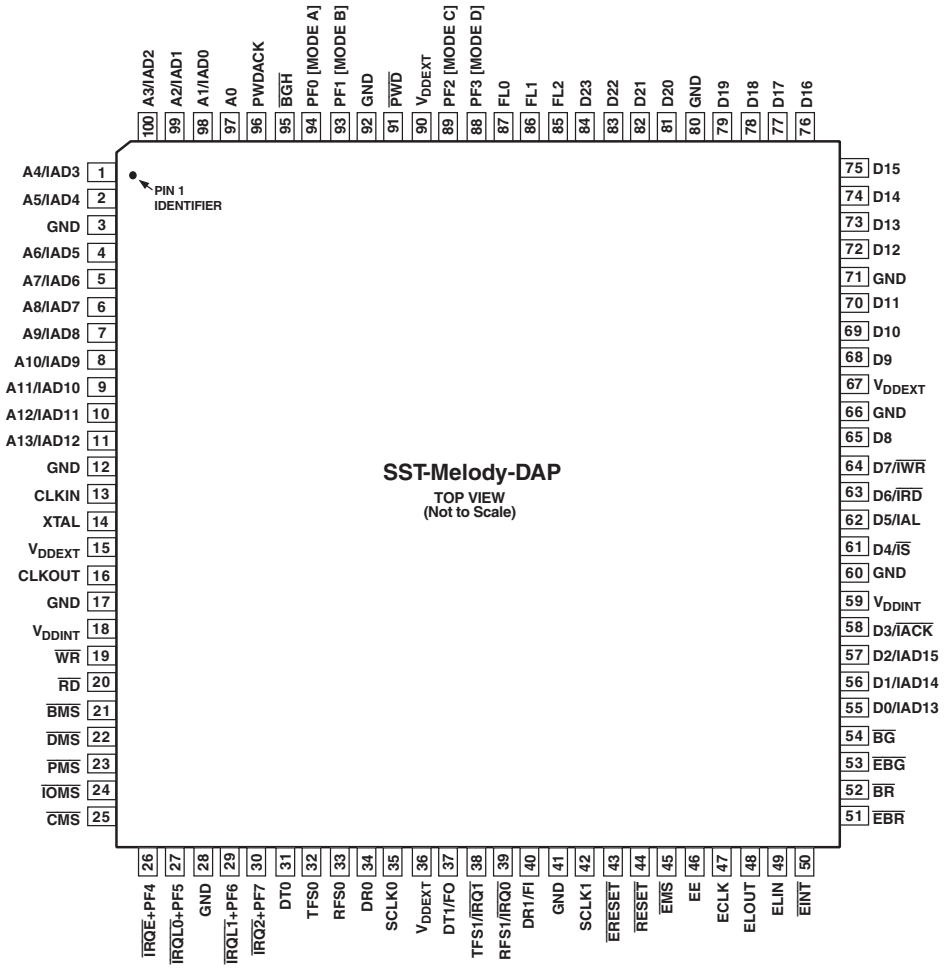
[3]Applies to output pins ($\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$)

ORDERING INFORMATION

The Analog Devices SST-Melody-DAP Reference Design must be ordered under the part number ADSST-Melody-SDK for the standalone reference design. This includes the evaluation board with an evaluation copy of the software and schematics.

Designers of products using this reference design also will be required to sign a license agreement with the respective license holder—i.e., Digital Theater Systems (DTS), Dolby Laboratories, THX Ltd., Microsoft, or SRS Labs—to use the appropriate code and produce proof to Analog Devices of having successfully completed the appropriate licensing procedures before final products can be shipped to them. The final product will be shipped from Analog Devices and will include the decoder chipset and software; customers will be required to sign license agreements with Analog Devices and separately pay system royalties to the respective license holder.

100-LEAD LQFP
PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SST-Melody-DAP features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

The LQFP package pinout is shown in the Pin Function Descriptions. Pin names in bold text replace the plain text named functions when Mode C = 1. A plus (+) sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of RESET.

The multiplexed pins DT1/FO, TFS1/$\overline{IRQ1}$, RFS1/$\overline{IRQ0}$, and DR1/FI are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
1	A4/IAD3	26	$\overline{IRQE}$+PF4	51	$\overline{EBR}$	76	D16
2	A5/IAD4	27	$\overline{IRQL0}$+PF5	52	$\overline{BR}$	77	D17
3	GND	28	GND	53	$\overline{EBG}$	78	D18
4	A6/IAD5	29	$\overline{IRQL1}$+PF6	54	$\overline{BG}$	79	D19
5	A7/IAD6	30	$\overline{IRQ2}$+PF7	55	D0/IAD13	80	GND
6	A8/IAD7	31	DT0	56	D1/IAD14	81	D20
7	A9/IAD8	32	TFS0	57	D2/IAD15	82	D21
8	A10/IAD9	33	RFS0	58	D3/$\overline{IACK}$	83	D22
9	A11/IAD10	34	DR0	59	V_{DDINT}	84	D23
10	A12/IAD11	35	SCLK0	60	GND	85	FL2
11	A13/IAD12	36	V_{DDEXT}	61	D4/$\overline{IS}$	86	FL1
12	GND	37	DT1/FO	62	D5/IAL	87	FL0
13	CLKIN	38	TFS1/$\overline{IRQ1}$	63	D6/$\overline{IRD}$	88	PF3 [MODE D]
14	XTAL	39	RFS1/$\overline{IRQ0}$	64	D7/$\overline{IWR}$	89	PF2 [MODE C]
15	V_{DDEXT}	40	DR1/FI	65	D8	90	V_{DDEXT}
16	CLKOUT	41	GND	66	GND	91	$\overline{PWD}$
17	GND	42	SCLK1	67	V_{DDEXT}	92	GND
18	V_{DDINT}	43	$\overline{ERESET}$	68	D9	93	PF1 [MODE B]
19	$\overline{WR}$	44	$\overline{RESET}$	69	D10	94	PF0 [MODE A]
20	$\overline{RD}$	45	$\overline{EMS}$	70	D11	95	$\overline{BGH}$
21	$\overline{BMS}$	46	EE	71	GND	96	PWDACK
22	$\overline{DMS}$	47	ECLK	72	D12	97	A0
23	$\overline{PMS}$	48	ELOUT	73	D13	98	A1/IAD0
24	$\overline{IOMS}$	49	ELIN	74	D14	99	A2/IAD1
25	$\overline{CMS}$	50	$\overline{EINT}$	75	D15	100	A3/IAD2

TIMING SPECIFICATIONS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, the user cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. There is no control over this. Timing circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics may be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY TIMING SPECIFICATIONS

Table I shows common memory device specifications and the corresponding SST-Melody-DAP timing parameters, for your convenience.

Table I. Memory Timing Specifications

Memory Device Specification	Parameter	Timing Parameter Definition*
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{xMS}$ Hold before $\overline{WR}$ Low
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
OE to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid

*$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, or $\overline{IOMS}$.

FREQUENCY DEPENDENCY FOR TIMING SPECIFICATIONS

t_{CK} is defined as 0.5 t_{CKI}. The SST-Melody-DAP uses an input clock with a frequency equal to half the instruction rate. For example, a 37.50 MHz input clock (which is equivalent to 26.6 ns) yields a 13.3 ns processor cycle (equivalent to 75 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 2 ns = 0.5 (15 ns) – 2 ns = 5.5 ns

Table II. Environmental Conditions*

Rating Description	Symbol	LQFP	Mini-BGA
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48°C/W	63.3°C/W
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50°C/W	70.7°C/W
Thermal Resistance (Junction-to-Case)	θ_{JC}	2°C/W	7.4°C/W

*Where the Ambient Temperature Rating (T_{AMB}) is:
$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^{\ 2} \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DDEXT} = 3.3 V and t_{CK} = 30 ns.

Total Power Dissipation = $P_{INT} + (C \times V_{DDEXT}^{\ 2} \times f)$

P_{INT} = internal power dissipation from Power vs. Frequency graph (see Figures 2a through 2c).

$(C \times V_{DDEXT}^{\ 2} \times f)$ is calculated for each output:

Table III. Power Dissipation Example

Parameter	No. of Pins	× C (pF)	× $V_{DDEXT}^{\ 2}$ (V)	× f (MHz)	PD (mW)
Address	7	10	3.3^2	16.67	12.7
Data Output, $\overline{WR}$	9	10	3.3^2	16.67	16.6
$\overline{RD}$	1	10	3.3^2	16.67	1.8
CLKOUT, $\overline{DMS}$	2	10	3.3^2	33.3	7.2
Total					38.2

Total power dissipation for this example is P_{INT} + 38.0 mW.

Output Drive Currents

Figure 1 shows typical I–V characteristics for the output drivers on the SST-Melody-DAP. The curves represent the current drive capability of the output drivers as a function of output voltage.

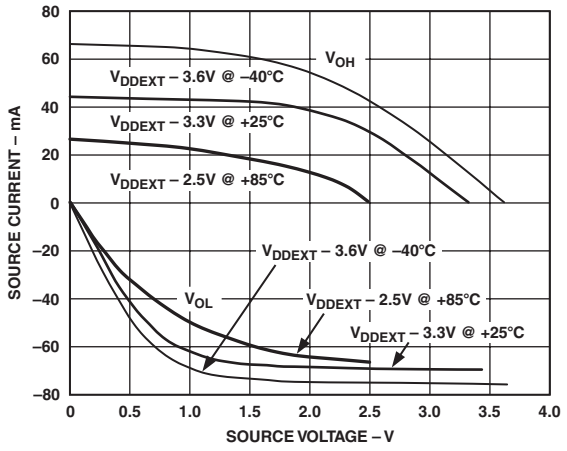
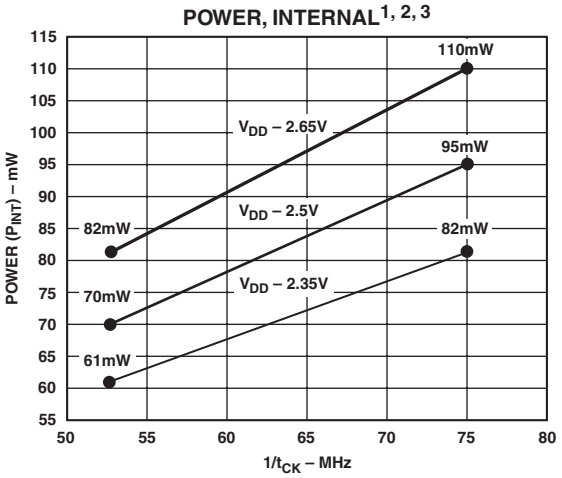
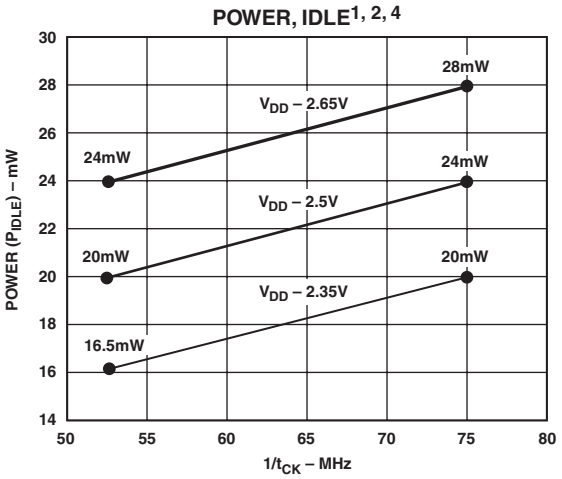
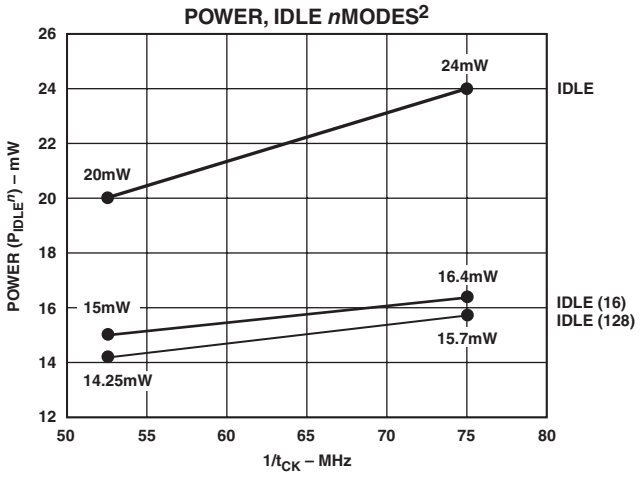


Figure 1. Typical Output Driver Characteristics







NOTES
VALID FOR ALL TEMPERATURE GRADES.
1 POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2 TYPICAL POWER DISSIPATION AT 2.5V V_{DIDINT} AND 25°C, EXCEPT WHERE SPECIFIED.
3 IDO MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 20% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
4 IDLE REFERS TO STATE OF OPERATING DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 2. Power vs. Frequency

Capacitive Loading

Figures 3 and 4 show the capacitive loading characteristics of the SST-Melody-DAP.

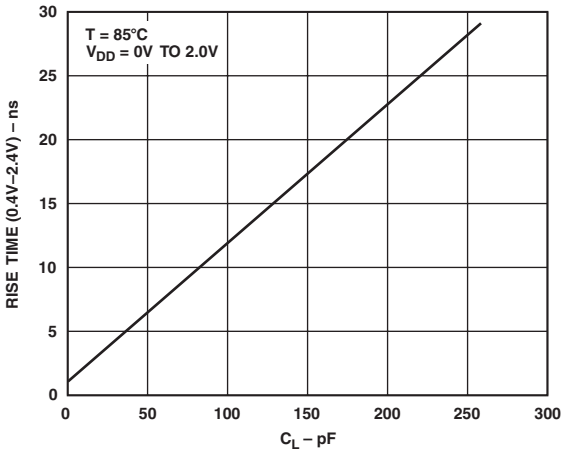


Figure 3. Typical Output Rise Time vs. Load Capacitance (at Maximum Ambient Operating Temperature)

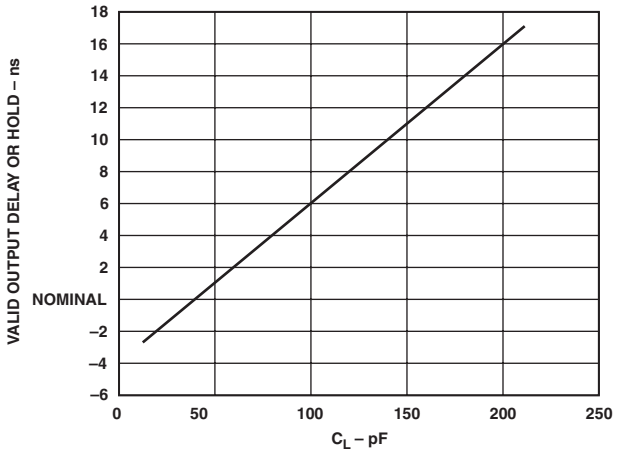


Figure 4. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

SST-Melody-DAP

SOFTWARE ARCHITECTURE

The SST-Melody-DAP software programming model has the following parts:

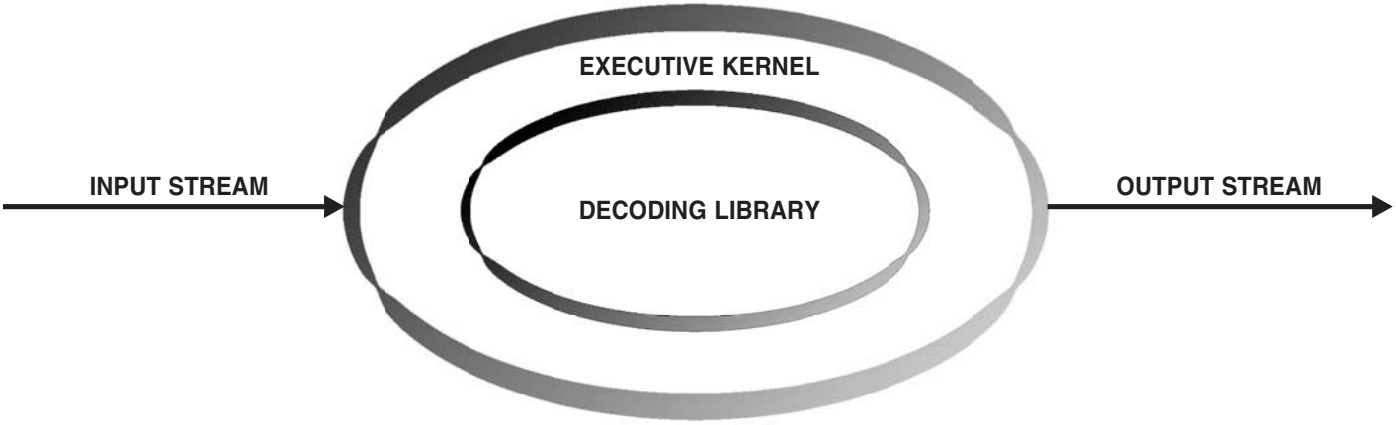
- Executive kernel
- Algorithm suite as library modules

The executive kernel has the following functions:

- Power-up hardware initialization
- Serial port management
- Automatic stream detect
- Automatic code load
- Command processing
- Interrupt handling
- Data buffer management
- Calling library module
- Status report

The executive kernel is executed as soon as booting takes place. The hardware resources are initialized in the beginning. The "command buffer" and general-purpose programmable flag pins are initialized. Various data buffers and memory variables are initialized. Interrupts are programmed and enabled. Then definite signatures are written "command buffer" to inform the host that ADSP is ready to receive the commands. Once commands are issued by host micro, these are executed and appropriate action takes place. Decoding is handled by issuing appropriate commands by host micro.

The kernel communicates with the library module for a particular algorithm in a definite way. The details are found in the specific implementation documents.



ARCHITECTURE OVERVIEW

The SST-Melody-DAP instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The SST-Melody-DAP assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

A functional block diagram of the SST-Melody-DAP is provided. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the SST-Melody-DAP executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is postmodified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip. The two databuses (PMD and DMD) share a single external databus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the SST-Melody-DAP to fetch two operands in a single cycle, one from program memory and one from data memory. The SST-Melody-DAP can fetch an operand from program memory and the next instruction in the same cycle. In lieu of the address and databus for external memory connection, the SST-Melody-DAP may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals (BR, BGH, and BG).

One execution mode (Go Mode) allows the SST-Melody-DAP to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted. The SST-Melody-DAP can respond to 11 interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port, and the power-down circuitry. There is also a master RESET signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The SST-Melody-DAP provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The SST-Melody-DAP incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the SST-Melody-DAP SPORTs:

- SPORTs are bidirectional and have a separate, double buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data-word lengths from three to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data-word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data-word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24- or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts (IRQ0 and IRQ1) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

PIN DESCRIPTIONS

The SST-Melody-DAP is available in a 100-lead LQFP package and a 144-ball mini-BGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt, and external bus pins have dual multiplexed functionality. The external bus pins are configured during RESET only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics.

Common-Mode Pins

Mnemonic	No. of Pins	I/O	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
$\overline{\text{IRQ2}}$ PF7	1	I I/O	Edge- or Level-Sensitive Interrupt Request[1] Programmable I/O Pin
$\overline{\text{IRQL1}}$ PF6	1	I I/O	Level-Sensitive Interrupt Requests[1] Programmable I/O Pin
$\overline{\text{IRQL0}}$ PF5	1	I I/O	Level-Sensitive Interrupt Requests[1] Programmable I/O Pin
$\overline{\text{IRQE}}$ PF4	1	I I/O	Edge-Sensitive Interrupt Requests[1] Programmable I/O Pin
Mode D PF3	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
Mode C PF2	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
Mode B PF1	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
Mode A PF0	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port I/O Pins
$\overline{\text{IRQ1}}$:$\overline{\text{IRQ0}}$, FI, FO			Edge- or Level-Sensitive Interrupts, FI, FO[2]
$\overline{\text{PWD}}$	1	I	Power-Down Control Input
PWDACK	1	O	Power-Down Control Output
FL0, FL1, FL2	3	O	Output Flags
V_{DDINT}	2	I	Internal V_{DD} (2.5 V) Power (LQFP)
V_{DDEXT}	4	I	External V_{DD} (2.5 V or 3.3 V) Power (LQFP)
GND	10	I	Ground (LQFP)
V_{DDINT}	4	I	Internal V_{DD} (2.5 V) Power (Mini-BGA)
V_{DDEXT}	7	I	External V_{DD} (2.5 V or 3.3 V) Power (Mini-BGA)
GND	20	I	Ground (Mini-BGA)
EZ-Port	9	I/O	For Emulation Use

NOTES
[1]Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, then the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices, or set as a programmable flag.
[2]SPORT configuration determined by the DSP System Control Register. Software configurable.

Memory Interface Pins

The SST-Melody-DAP processor can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C Pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running.

The following tables list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinout tables.

Full Memory Mode Pins (Mode C = 0)

Mnemonic	No. of Pins	I/O	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses)

Host Mode Pins (Mode C = 1)

Mnemonic	No. of Pins	I/O	Function
IAD15:0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access*
D23:8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

*In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

Table IV. Pin Terminations[1, 2, 3, 4]

Table IV shows the recommendations for terminating unused pins.

Mnemonic	I/O Three-State (Z)	Reset State	Hi-Z[5] Caused By	Unused Configuration
XTAL	I	I		Float
CLKOUT	O	O		Float
A13:1 or IAD 12:0	O (Z) I/O (Z)	Hi-Z Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$ $\overline{\text{IS}}$	Float Float
A0	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
D23:8 D7 or	I/O (Z) I/O (Z)	Hi-Z Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$ $\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float Float
$\overline{\text{IWR}}$	I	I		High (Inactive)
D6 or $\overline{\text{IRD}}$	I/O (Z) I	Hi-Z I	$\overline{\text{BR}}$, $\overline{\text{EBR}}$ $\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float High (Inactive)
D5 or IAL	I/O (Z) I	Hi-Z I		Float Low (Inactive)
D4 or $\overline{\text{IS}}$	I/O (Z) I	Hi-Z I	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float High (Inactive)
D3 or $\overline{\text{IACK}}$	I/O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float Float
D2:0 or IAD15:13	I/O (Z) I/O (Z)	Hi-Z Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$ $\overline{\text{IS}}$	Float Float

Table IV. Pin Terminations (continued)

Mnemonic	I/O Three-State (Z)	Reset State	Hi-Z[5] Caused By	Unused Configuration
$\overline{\text{PMS}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{DMS}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{BMS}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{IOMS}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{CMS}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{RD}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{WR}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{BR}}$	I	I		High (Inactive)
$\overline{\text{BG}}$	O (Z)	O	EE	Float
$\overline{\text{BGH}}$	O	O		Float
$\overline{\text{IRQ2}}$/PF7	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{\text{IRQL1}}$/PF6	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{\text{IRQL0}}$/PF5	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{\text{IRQE}}$/PF4	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	I		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{\text{IRQ0}}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{\text{IRQ1}}$	I/O	I		High or Low
DT1/FO	O	O		Float
EE	I	I		Float
$\overline{\text{EBR}}$	I	I		Float
$\overline{\text{EBG}}$	O	O		Float
$\overline{\text{ERESET}}$	I	I		Float
$\overline{\text{EMS}}$	O	O		Float
$\overline{\text{EINT}}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

NOTES
[1]If the CLKOUT Pin is not used, turn it off using CLKODIS in SPORT0 autobuffer control register.
[2]If the interrupt/programmable flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins high (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1 prior to enabling interrupts, and let pins float.
[3]All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
[4]CLKIN, RESET, and PF3:0/MODE D:A are not included in the table because these pins must be used.
[5]Hi-Z = High impedance.

Interrupts

The interrupt controller allows the processor to respond to the 11 possible interrupts and reset with minimum overhead. The SST-Melody-DAP provides four dedicated external interrupt input pins: $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, and $\overline{IRQE}$ (shared with the PF7:4 Pins). In addition, SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, FI, and FO, for a total of six external interrupts. The SST-Melody-DAP also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and $\overline{RESET}$). The $\overline{IRQ2}$, $\overline{IRQ0}$, and $\overline{IRQ1}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{IRQL0}$ and $\overline{IRQL1}$ are level-sensitive and $\overline{IRQE}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table V.

Table V. Interrupt Priority and Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0000 (Highest Priority)
Power-Down (Nonmaskable)	002C
$\overline{IRQ2}$	0004
$\overline{IRQL1}$	0008
$\overline{IRQL0}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{IRQE}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or $\overline{IRQ1}$	0020
SPORT1 Receive or $\overline{IRQ0}$	0024
Timer	0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The SST-Melody-DAP masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$ external interrupts to be either edge or level-sensitive. The $\overline{IRQE}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{IRQL0}$ and $\overline{IRQL1}$ pins are external level-sensitive interrupts. The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

ENA INTS;

DIS INTS;

When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

The SST-Melody-DAP has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT Pin may also be disabled to reduce external power dissipation.

Power-Down

The SST-Melody-DAP processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle startup.
- Power-down is initiated by either the Power-Down pin (PWD) or the software Power-Down Force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{RESET}$ pin also can be used to terminate power-down.
- Power-Down Acknowledge pin indicates when the processor has entered power-down.

Idle

When the SST-Melody-DAP is in the Idle mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode, IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on the SST-Melody-DAP to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

IDLE (n);

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals

(such as SCLK, CLKOUT) and timer clock are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, the SST-Melody-DAP will remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster than can be serviced rate, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 5 shows typical basic system configurations with the SST-Melody-DAP, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. The SST-Melody-DAP also provides four external interrupts and two serial ports or six external interrupts and one serial port.

Host Memory mode allows access to the full external databus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

Clock Signals

The SST-Melody-DAP can be clocked by either a crystal or a TTL compatible clock signal. The CLKIN input cannot be halted, changed during operation, nor operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state.

If an external clock is used, it should be a TTL compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input must be left unconnected.

The SST-Melody-DAP uses an input clock with a frequency equal to half the instruction rate; a 37.50 MHz input clock yields a 13 ns processor cycle (which is equivalent to 75 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the SST-Melody-DAP includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 6. Capacitor values are dependent

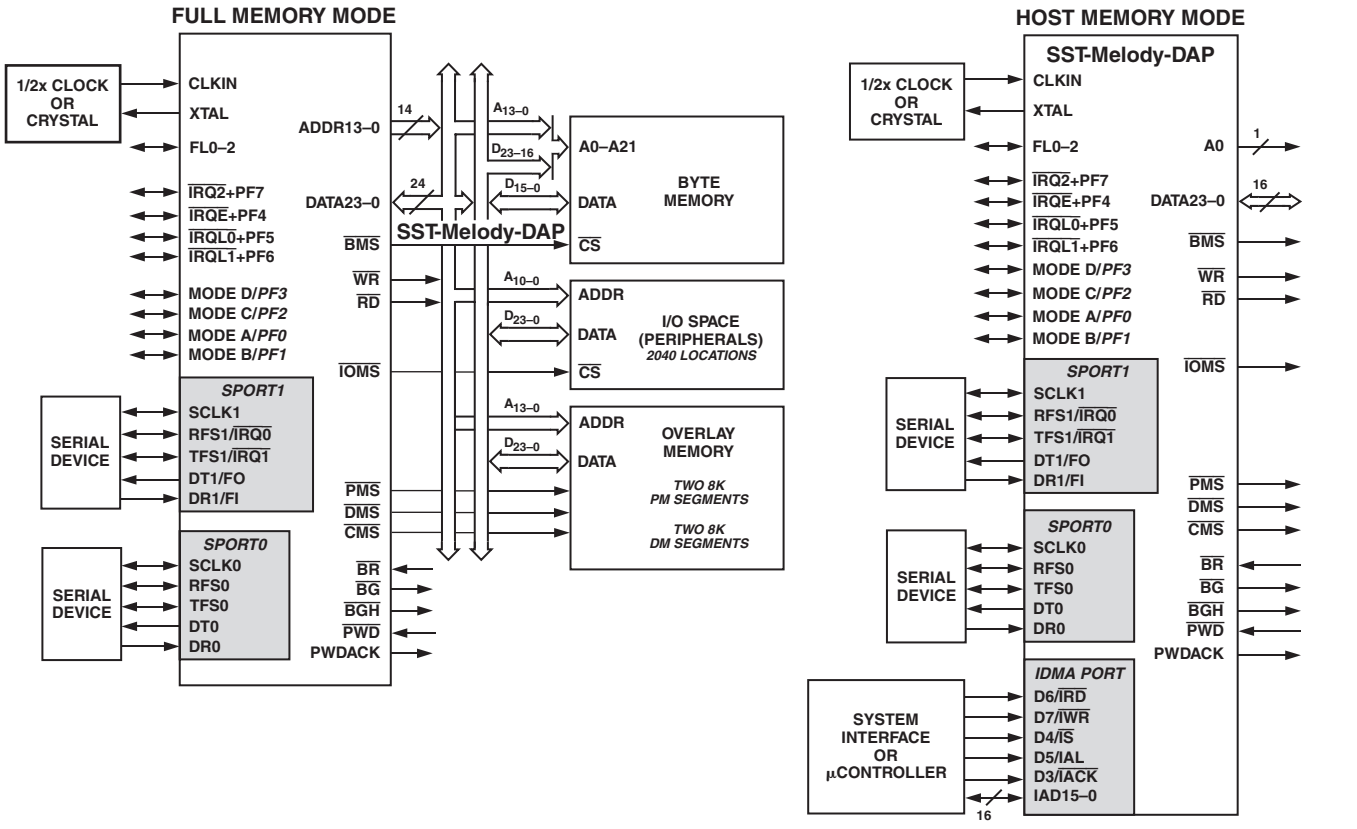


Figure 5. Basic System Interface

on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control register.

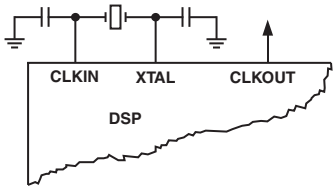


Figure 6. External Crystal Connections

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ signal initiates a master reset of the SST-Melody-DAP. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization.

$\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time. The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid VDD is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence, the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulsewidth specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, the use of an external Schmitt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

Power Supplies

The SST-Melody-DAP has separate power supply connections for the internal (VDDINT) and external (VDDEXT) power supplies. The internal supply must meet the 2.5 V requirement. The external supply can be connected to either a 2.5 V or 3.3 V supply. All external supply pins must be connected to the same supply. All input and I/O pins can tolerate input voltages up to 3.6 V, regardless of the external supply voltage. This feature provides maximum flexibility in mixing 2.5 V and 3.3 V components.

MODES OF OPERATION

Setting Memory Mode

Memory Mode selection for the SST-Melody-DAP is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power

Table VI. Modes of Operation

Mode D	Mode C	Mode B	Mode A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory mode.*
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host mode; $\overline{\text{IACK}}$ has active pull-down (requires additional hardware).
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host mode. $\overline{\text{IACK}}$ has active pull-down.*
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host mode; $\overline{\text{IACK}}$ requires external pull-down (requires additional hardware).
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host mode. $\overline{\text{IACK}}$ requires external pull down.*

*Considered standard operating settings. Using these configurations allows for easier design and better memory management.

consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state, and will not switch.

Active Configuration

Active configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's RESET signal such that it only drives the PF2 pin when RESET is active low. When RESET is deasserted, the driver should three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level and will not oscillate should the three-state driver's level hover around the logic switching point.

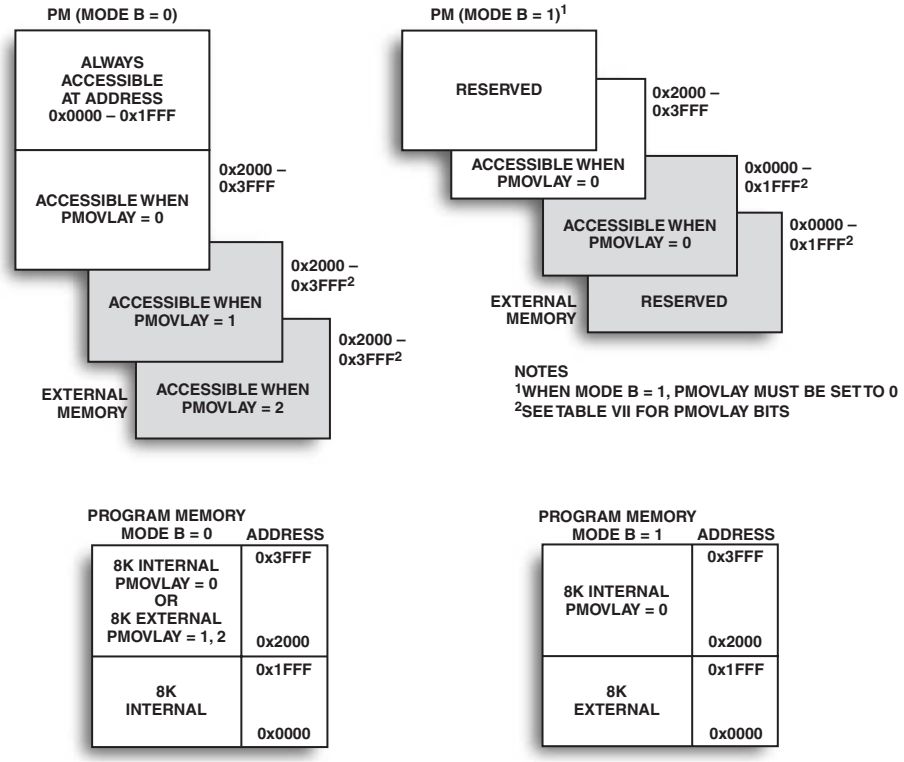


Figure 7. Program Memory

Table VII. PMOVLAY Bits

PMOVLAY	Memory	A13	A12:0
0	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address between 0x2000 and 0x3FFF

$\overline{\text{IACK}}$ Configuration

Mode D = 0 and in Host Mode, $\overline{\text{IACK}}$ is an active, driven signal and cannot be "Wire-Ored."

Mode D = 1 and in Host Mode, $\overline{\text{IACK}}$ is an open drain and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be "Wire-Ored" together.

MEMORY ARCHITECTURE

The SST-Melody-DAP provides a variety of memory and peripheral interface options. The key functional groups are program memory, data memory, byte memory, and I/O. Refer to the following figures and tables for PM and DM memory allocations in the SST-Melody-DAP.

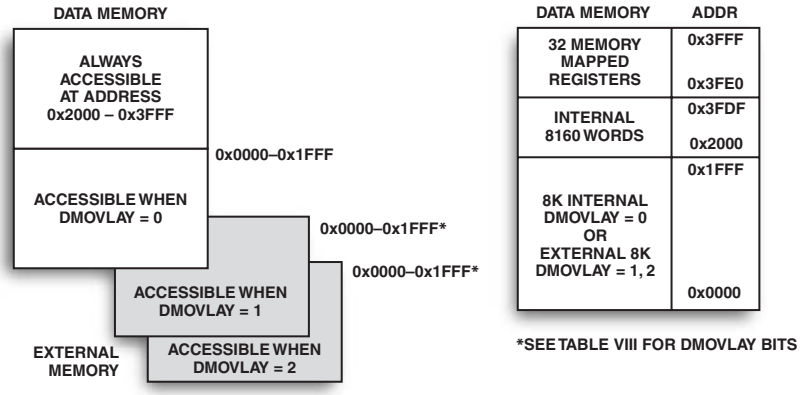


Figure 8. Program Memory

Table VIII. DMOVLAY Bits

DMOVLAY	Memory	A13	A12:0
0	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address between 0x2000 and 0x3FFF

Program Memory

Program memory (Full Memory mode) is a 24-bit wide space for storing both instruction opcodes and data. The SST-Melody-DAP has 16K words of program memory RAM on-chip, and the capability of accessing up to two 8K external memory overlay spaces using the external databus.

Program memory (Host mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in Host Mode due to a restricted databus that is 16 bits wide only.

Data Memory

Data memory (Full Memory mode) is a 16-bit wide space used for the storage of data variables and for memory-mapped control registers. The SST-Melody-DAP has 16K words on data memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external databus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register and the Wait State mode bit.

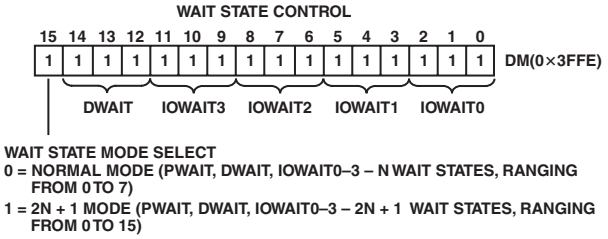


Figure 9. Wait State Control Register

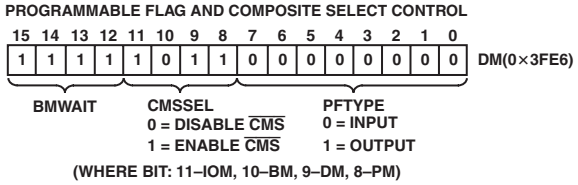


Figure 10. Programmable Flag and Composite Control Register

Memory-Mapped Registers (New to the SST-Melody-DAP)
The SST-Melody-DAP has three memory-mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the SST-Melody-DAP's wait state and BMS control features. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a gray field. These bits should always be written with zeros.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

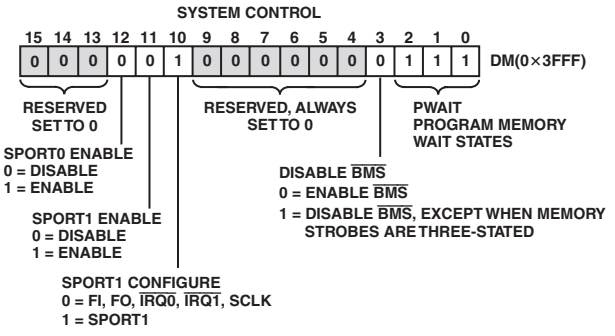


Figure 11. System Control Register

I/O Space (Full Memory Mode)
The SST-Melody-DAP supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower 11 bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0–3, which in combination with the wait state mode bit specify up to 15 wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table IX.

Table IX. Wait States

Address Range	Wait State Register
0x000–1x1FF	IOWAIT0 and Wait State Mode Select Bit
0x200–3x1FF	IOWAIT1 and Wait State Mode Select Bit
0x400–5x1FF	IOWAIT2 and Wait State Mode Select Bit
0x600–7x1FF	IOWAIT3 and Wait State Mode Select Bit

Composite Memory Select ($\overline{\text{CMS}}$)
The SST-Melody-DAP has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the CMS Pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The CMS pin functions like the other memory select signals with the same timing and bus request logic. A "1" in the enable bit causes the assertion of the CMS signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Byte Memory Select ($\overline{\text{BMS}}$)
The SST-Melody-DAP's $\overline{\text{BMS}}$ disable feature, combined with the CMS pin, allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$ select, and an SRAM could be connected to CMS. Because $\overline{\text{BMS}}$ is enabled at reset, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the CMS signal to respond to $\overline{\text{BMS}}$, enabling the SRAM.

Byte Memory
The byte memory space is a bidirectional, 8-bit wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8. The byte memory space on the SST-Melody-DAP supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register and the Wait State Mode bit.

Byte Memory DMA (BDMA, Full Memory Mode)
The byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16-, or 24-bit word transferred.

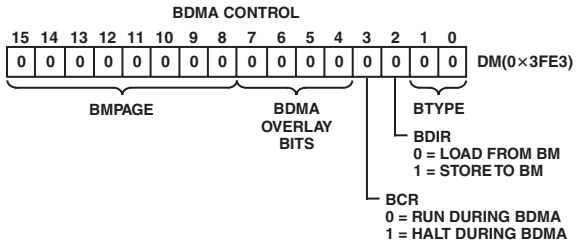


Figure 12. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table X shows the data formats supported by the BDMA circuit.

Table X. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value, the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

The BDMA Overlay bits specify the OVLAY memory blocks to be accessed for internal memory. For SST-Melody-DAP, set to zero BDMA Overlay bits in the BDMA Control register.

The BMWAIT field, which has four bits on SST-Melody-DAP, allows selection up to 15 wait states for BDMA transfers.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)
The IDMA port provides an efficient means of communication between a host system and the SST-Melody-DAP. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the value of Bits 7:0 represent the IDMA overlay and bits 14:8 must be set to 0. If Bit 15 = 0, the value of Bits 13:0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access. For SST-Melody-DAP, IDDMOVLAY and IDPMOVLAY bits in the IDMA Overlay register should be set to zero.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks IACK line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

The IDMA port has a 16-bit multiplexed address and databus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the SST-Melody-DAP is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal ($\overline{\text{IS}}$) latches this value into the IDMAA register.

Once the address is stored, data can be read from or written to, the SST-Melody-DAP's on-chip memory. Asserting the select line ($\overline{\text{IS}}$) and the appropriate read or write line ($\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ respectively) signals the SST-Melody-DAP that a particular transaction is required. In either case, there is a one processor cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{\text{IS}}$) and address latch enable (IAL) directs the SST-Melody-DAP to write the address onto the IAD0–14 bus into the IDMA control register. If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, shown in Figure 13, is memory-mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. For SST-Melody-DAP, IDDMOVLAY and IDPMOVLAY bits in the IDMA overlay register should be set to 0.

Refer to the following figures for more information on IDMA and DMA memory maps.

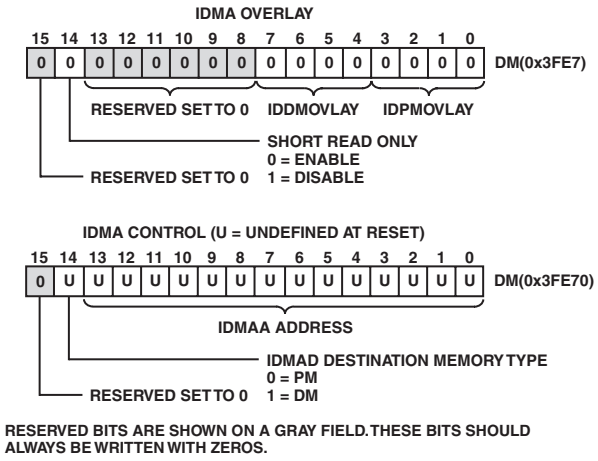


Figure 13. IDMA Control/OVLAY Registers

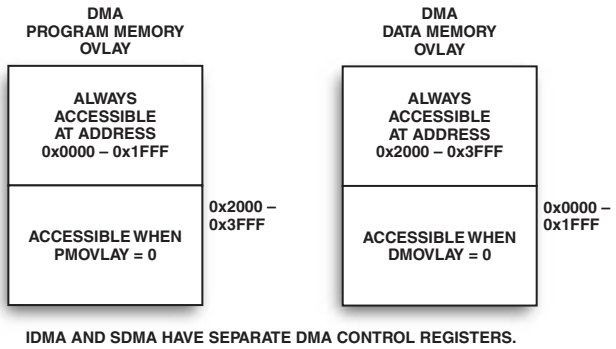


Figure 14. Direct Memory Access—PM and DM Memory Maps

Bootstrap Loading (Booting)
The SST-Melody-DAP has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B, and C Configuration bits.

When the MODE pins specify BDMA booting, the SST-Melody-DAP initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at Address 0.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host mode, the addresses to boot memory must be constructed externally to the SST-Melody-DAP. The only memory address bit provided by the processor is A0.

IDMA Port Booting
The SST-Melody-DAP can also boot programs through its Internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the SST-Melody-DAP boots from the IDMA port. The IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

Bus Request and Bus Grant
The SST-Melody-DAP can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the SST-Melody-DAP is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, and $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go mode is enabled, the SST-Melody-DAP will not halt program execution until it encounters an instruction that requires an external memory access.

If the SST-Melody-DAP is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The BGH pin is asserted when the SST-Melody-DAP requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting the bus request. Once the bus is released, the SST-Melody-DAP deasserts BG and BGH and executes the external memory access.

Flag I/O Pins
The SST-Melody-DAP has eight general-purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction: 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the SST-Melody-DAP's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

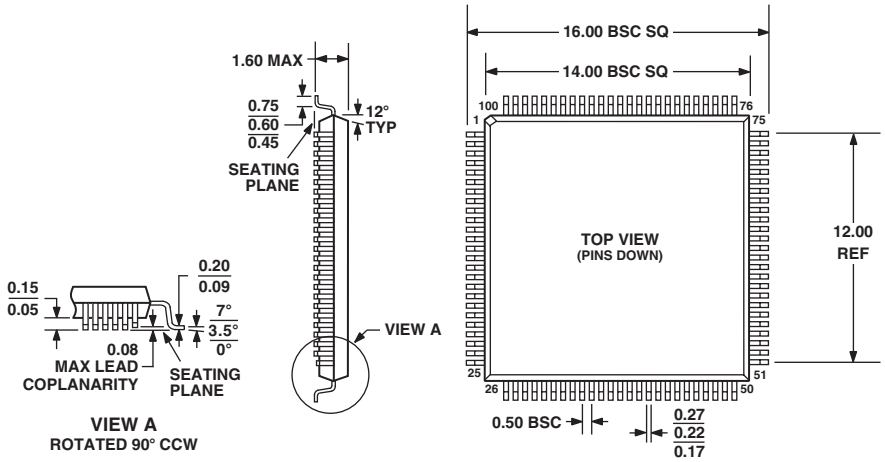
In addition to the programmable flags, the SST-Melody-DAP has five fixed-mode flags, FI, FO, FL0, FL1, and FL2. FL0–FL2 are dedicated output flags. FI and FO are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

OUTLINE DIMENSIONS

Dimensions shown in millimeters

100-Lead Quad Flatpack [LQFP]
(ST-100)



COMPLIANT TO JEDEC STANDARDS MS-026BED

THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 OF ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION

C03010–0–10/02(0)

PRINTED IN U.S.A.